What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of reducing power consumption in a memory integrated circuit comprising:
receiving a clock signal at an input of a signal delay device;
delaying propagation of said signal within said signal delay device to create a delayed signal;
receiving said delayed signal at a clock input of a data buffer; and
selectively preventing said input of said signal delay device from receiving said clock signal.

2. A method as defined in claim 1 wherein said signal delay device comprises a delay locked loop.

3. A method as defined in claim 1 wherein said data buffer comprises a data output buffer.

4. A method as defined in claim 1 wherein said step of preventing the input of said signal delay device from receiving said clock signal further comprises controlling a gate to interrupt transmission of said clock signal.

5. A method of reducing power consumption in a memory device comprising:
receiving a free running clock signal;
using said received clock signal for clocking an input of a delay locked loop;
using an output of said delay locked loop to transfer data out of said memory device; and

interrupting the supply of said received clock signal to said delay locked loop during a power down operation of said memory device.

6. A method as defined in claim 5 further comprising:

operating a switch with a control signal to cause it to permit or arrest passage of said received clock signal to said delay locked loop.

7. A memory integrated circuit comprising:

a data buffer having a clock input;

a signal delay device having a clock output and a clock input; said delay device clock output being operatively connected to said data buffer clock input; and a switch operatively connected between a clock source and said delay device clock input.

8. A memory integrated circuit as defined in claim 7 wherein said signal delay device further comprises a delay locked loop, including a plurality of delay elements.

9. A method of reducing power consumption in a memory integrated circuit having a delay locked loop comprising:

using a free running external clock signal to drive an input of a delay locked loop during a first power up time period; and

arresting the clock signal during a second power down time period, such that said input receives no external clock signal during said second time period.

10. A method as defined in claim 9 wherein said step of arresting the clock signal includes operating a switch to prevent said clock signal from reaching said input.

11. A method as defined in claim 9 wherein said switch is a transistor based logic gate circuit.

12. A memory integrated circuit comprising:
a delay locked loop having a clock input; a transistor based switch operatively connected between a clock source and said clock input; said transistor based switch including a control input adapted to cause said switch to interrupt passage of a clock signal from said source to said clock input.

13. A memory integrated circuit as defined in claim 12 wherein said clock source is external to said memory integrated circuit.

14. A memory integrated circuit as defined in claim 12 further comprising a power down mode control device for operating said switch.

15. A random access memory circuit having reduced power consumption in power down mode comprising:

first and second data paths; a data buffer operatively connected between said first and second data paths, said data buffer having a clock input;

a signal delay device, having a clock input and a clock output; said delay device clock output being operatively connected to said data buffer clock input;

a switch having a clock input, a clock output, and a control input;

said switch clock input being connected to receive an external clock signal;

said switch clock output being operatively connected to said signal delay device clock input;

said switch control input being connected to receive a power down signal, and adapted to prevent passage of said external clock signal to said signal delay device on receipt of said power down signal;

16. A random access memory circuit as defined in claim 15 wherein said signal delay device further comprises a delay locked loop circuit, including a plurality of delay elements.

17. An electronic system comprising:

an external clock; a memory integrated circuit including a delay locked loop having an external clock input; a logic gate circuit operatively connected between said external clock and said external clock input; said gate circuit including a control input adapted to cause said gate circuit to interrupt passage of an external clock signal from said source to said external clock input; a control device adapted to signal a power down mode to said control input of said gate circuit; and a power supply operatively connected to said external clock, said memory integrated circuit, and said control device.